

ABSTRACT

A new method to design and verify a multi-power integrated circuit device is achieved. A multi-power gate-level netlist is provided. This multi-power gate-level netlist includes multi-power net information. This multi-power gate-level netlist is translated to thereby create a non-multi-power gate-level netlist. This translating comprises removing the multi-power net information. Circuit cells are then placed and routed to create a physical view of the multi-power integrated circuit device. This placing and routing step uses the non-multi-power gate-level netlist. Text labels for the multi-power net information are attached to the physical view. The physical view and the multi-power gate-level netlist are compared to verify the correctness of the physical view and to complete the design and verification of the multi-power integrated circuit device.